

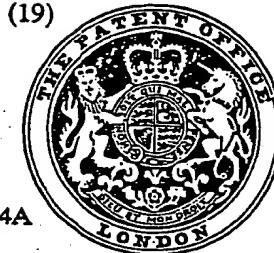
## PATENT SPECIFICATION

(11)

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(21) Application No. 38062/77 (22) Filed 13 Sep. 1977 (1)  
(31) Convention Application No. 2641302 (32) Filed 14 Sep. 1976 in  
(33) Fed. Rep. of Germany (DE)  
(44) Complete Specification Published 28 Mar. 1979  
(51) INT. CL.<sup>2</sup> H01L 29/78  
(52) Index at Acceptance  
H1K 1CA 4C11 4C14 4C14A 4H1A 4H1C 4H3X 9B4A  
9D1 9E 9F 9N2 9N3 9P1 9R2 CAX



(54) IMPROVEMENTS IN OR RELATING TO FIELD-EFFECT TRANSISTORS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The present invention relates to n-channel insulating layer field-effect transistors.

Integrated circuits provided with MIS-transistors are currently frequently constructed in epitaxial layers arranged on an insulating substrate. For this purpose, an epitaxial silicon layer is deposited on a monocrystalline insulating substrated, e.g. of sapphire or spinel. Doped zones are then produced in this epitaxial silicon layer in accordance with the particular type of semiconductor component to be produced. A disadvantage of this technique is that, as a result of lattice variations between the substrate and the epitaxial layer positively charged surface states occur which induce an n-conducting zone in the epitaxial silicon layer in the vicinity of the substrate surface. This n-conducting zone has a thickness equal to a Debye-length and is thus about 5 nm thick. An n-conducting zone of this type at the substrate surface has a disadvantageous effect on the electrical behaviour of a field-effect transistor, for example, which consists of n<sup>+</sup>-conducting source and drain zones and an interlying n-conducting channel zone, since this induced n-conducting zone forms a further disturbing channel between the source and the drain which leads to a high blocking current for the field-effect transistor (see Appl. Phys. Letters 11, (1967), pages 132 to 134). This blocking current can be suppressed by introducing dopant into the induced zone of the epitaxial silicon layer by ion implantation, so as to reduce the conductivity of the induced zone. The concentration of the boundary surface states

which produce the induced zone fluctuate very considerably, however. The implantation doping used for compensation purposes must therefore be such that it serves to compensate for the effect of even the greatest possible concentration of boundary surface states. The strength of the implantation doping required is then, however, already such that the gradient of the field-effect transistor characteristic is considerably reduced.

It is an object of the present invention to provide an insulating field-effect transistor constructed in an epitaxial silicon layer on an insulating substrate and which has a low blocking current and a high transistor characteristic gradient.

According to the invention, there is provided an n-channel insulating layer field-effect transistor comprising an n-doped source zone, an n-doped drain zone and a weakly doped p-doped channel zone formed in an epitaxial silicon layer on an insulating substrate, wherein a strongly p-doped zone containing implanted p-dopant is located in said epitaxial layer in contact with the surface of said substrate, within a portion of the epitaxial layer adjacent to said source zone, a part of the concentration maximum of implanted dopant ions in said p-doped zone being located at a distance from the substrate surface which is a multiple of the Debye-length in said channel zone, said p-doped zone acting to interrupt any interference channel present in said epitaxial layer adjacent to the substrate boundary so as to electrically separate said source zone therefrom by a p-n boundary layer.

The invention is based on the realisation that, in order to reduce the blocking current produced by the boundary surface states, it is sufficient to interrupt the conductive interference channel which is induced by these states and which is present at the substrate surface, so that a conductive

connection is no longer established between the source and the drain via this interference channel, and that it is unnecessary to compensate by implantation for the entire n-conducting zone induced by the boundary surface states.

In accordance with the invention therefore, the zone of the epitaxial silicon layer which is provided with implanted dopant particles does not extend over the entire surface used for the insulating layer field-effect transistor as in previously known techniques, but is limited to a portion of the epitaxial silicon layer which includes the source zone. In the transistor according to the invention, the interference channel is interrupted by ensuring that the concentration of the implanted dopant ions in the implanted zone is such that a p-n boundary layer is present between this implanted zone and the n-conducting interference channel. This p-n boundary layer forms an electrical barrier by means of which the n-conducting interference channel which was originally produced as a result of boundary surface states and which is present adjacent the substrate surface is now interrupted. The implanted zone can underly and extend laterally of the source zone, or it can be of annular shape and surround the source zone. In a MOS-transistor which is constructed in an insular semiconductor layer, it is sufficient if the implanted zone lies adjacent to but spaced from the source zone and extends to both opposite ends of the island, and thus cuts off the source zone from the interference channel. The known insulating layer field-effect transistor can be regarded as a transistor which, in addition to the gate electrode arranged on the insulating layer, possesses a further "gate electrode" constituted by the surface of the insulating substrate which is provided with the boundary surface states. In the known field-effect transistor, the implantation doping which extends over the entire epitaxial layer virtually switches the additional "gate electrode" to zero potential, and consequently reduces the gradient of the characteristic of the field-effect transistor. In comparison, in a field-effect transistor in accordance with the invention, the gradient of this field-effect transistor is not fundamentally affected by the implantation doping.

In a preferred embodiment of the transistor of the invention, in the implanted doped zone, the concentration maximum of the implanted ions lies within a distance of 100 nm from the substrate surface. Preferably, the concentration of the implanted dopant ions in this region is between  $2 \times 10^{16}$  and  $2 \times 10^{17}$  ions per  $\text{cm}^3$ .

The transistor of the invention can advantageously be prepared by selectively doping

to form the doped zone by means of ion implantation carried out not over the whole of the semiconductor regions of the insulating layer field-effect transistor, but merely in that region including the source zone and a part of the channel on the source side. The implantation doping is effected through a mask which leaves uncovered that part of the field-effect transistor which is to be implanted, i.e. the source zone and a part of the channel zone adjacent thereto. The mask may consist, for example, of a photolacquer. The implantation doping is carried out with an ion energy such that the distribution maximum of the implanted dopant ions lies immediately above the boundary surface between the silicon layer and the insulating substrate.

The invention will now be further described with reference to the drawing, in which:

*Figure 1* is a schematic side-sectional view of one embodiment of the invention;

*Figure 2* is a schematic side-sectional view of a second embodiment of the invention; and

*Figure 3* is a similar view to that of *Figure 1*, to illustrate the production of the field-effect transistor of *Figure 1*.

Referring to *Figure 1*, on a monocrystalline substrate 1, which consists of sapphire ( $\text{Al}_2\text{O}_3$ ), there is arranged an epitaxial silicon layer 2 which is doped to be p-conducting with a basic doping of  $10^{14} - 5 \times 10^{15}$  per  $\text{cm}^3$ . In this epitaxial silicon layer, there are arranged a highly n-doped drain zone 3 and a likewise highly doped source zone 4. The channel zone 5 between them has the original doping of the layer 2. At the boundary surface 6 between the insulating substrate 1 and the epitaxial silicon layer 2, the insulating substrate contains boundary surface states 7 which are positively charged. These positive states 7 induce an interference channel 8 in the layer 2 adjacent the boundary surface 6 which contains conductivity electrons and thus is n-conductive. The source zone 4 and that part of the channel zone 5 which adjoins the source zone is crossed adjacent the boundary surface 6 by a zone 9 which contains implanted dopant ions, e.g. boron ions. This zone 9 does not extend as far as the drain zone 3 but is limited to a region 21 which underlies and extends laterally of the source zone 4. This region 21 extends no further than about m beyond the lateral boundaries of the source zone. The dopant concentration of the zone 9 is sufficiently high for it to be strongly p-doped. The concentration maximum of the implanted ions runs along a line 10 a part of which lies parallel to and at a distance of about 100 nm from the substrate surface 6. The zone 9 is electrically isolated by the boundary layer of a p-n junction 11 both from the remaining part of the surface zone 130

4 and from the n-conducting interference  
channel 8. The result of this is that the source  
zone 4 is no longer conductively connected to  
the interference channel 8, since the interfer-  
ence channel is cut by the p-n junction 11. At  
5 the surface of the epitaxial silicon layer, an  
insulating layer 12 consisting of silicon  
dioxide is arranged above the channel zone 5  
and on this an aluminium layer is arranged  
10 as a gate electrode 13 above the channel zone  
5. The insulating layer 12 contains windows  
through which conductor paths 14 and 15  
lead to the source zone 4 and the drain zone 3  
15 respectively and thus form electric contacts  
therewith.

In the embodiment illustrated in Figure 2,  
20 the field-effect transistor is formed in an  
island of weakly p-doped semiconductor  
material produced by etching from the  
epitaxial layer 2. The n<sup>+</sup>-doped source zone  
25 4 and drain zone 3 are formed at opposite  
sides of the island. The induced n-doped  
interference channel 8 adjacent the substrate  
1 is interrupted by a p-doped zone 9 which,  
in this example lies adjacent to but spaced  
from the source zone 4, and extends to both  
ends of the island.

The production of the transistor in  
30 accordance with the invention shown in  
Figure 1 is schematically illustrated in Figure  
3. A weakly p-doped silicon layer 2 is first  
deposited epitaxially onto an insulating sub-  
strate which in the example under consider-  
35 ation consists of sapphire. Individual islands  
may, if desired, be etched out of this layer as  
in the embodiment of Figure 2. In the  
epitaxial silicon layer 2, a highly n-doped  
source zone 4 and drain zone 3 are produced,  
40 e.g. by diffusing-in phosphorus. The epitax-  
ial silicon layer 2 is then covered by an  
electrically insulating layer 12 which may  
consist, for example, of silicon dioxide or of  
silicon nitride. A photolacquer layer 20 is  
45 then deposited onto this insulating layer 12.  
The photolacquer layer 20 is then exposed  
through a photo-mask and developed to  
form a window 31 in the photolacquer layer;  
this window is located above the source zone  
50 4 but has an area which is larger than that of  
the source zone. Implantation of p-dopant  
ions 22, e.g. boron ions, is then carried out,  
the photolacquer layer 20 serving as an  
implantation mask. The energy of the ions  
55 22 used is such that in the epitaxial silicon  
layer 2, the concentration maximum of the  
implanted ions runs along a line 10, a part of  
which lies parallel to and at a distance of  
about 0.1 μm from the surface 6 of the  
60 insulating substrate, which is a multiple of  
the Debye length in channel zone 5. The  
implantation is carried out with an overall  
dosage of from 2 x 10<sup>12</sup> to 5 x 10<sup>12</sup> per cm<sup>2</sup>.  
Subsequently, the photolacquer 20 is remov-  
65 ed and windows are etched into the  
insulating layer 12 for the subsequent

application of the source and drain contacts  
14 and 15 respectively, and these contacts  
and the gate electrode 13 are formed by  
vapour deposition through a mask.

#### WHAT WE CLAIM IS:-

1. An n-channel insulating layer field-  
effect transistor comprising an n-doped  
source zone, an n-dope drain zone and a  
weakly p-doped channel zone formed in an  
epitaxial silicon layer on an insulating  
substrate, wherein a strongly p-doped zone  
containing implanted p-dopant is located in  
said epitaxial layer in contact with the  
surface of said substrate, within a portion of  
the epitaxial layer adjacent to said source  
zone, a part of the concentration maximum  
of implanted dopant ions in said p-doped  
zone being located at a distance from the  
substrate surface which is a multiple of the  
Debye-length in said channel zone, said  
p-doped zone acting to interrupt any inter-  
ference channel present in said epitaxial layer  
adjacent to the substrate boundary so as to  
electrically separate said source zone there-  
from by a p-n boundary layer. 70

2. A field-effect transistor as claimed in  
Claim 1, wherein said p-doped zone extends  
laterally of said source zone. 75

3. A field-effect transistor as claimed in  
Claim 2, wherein said p-doped zone extends  
laterally of said source zone by at most 80

4. A field-effect transistor as claimed in  
any one of Claims 1 to 3, wherein the  
concentration maximum of the implanted  
dopant ions in said p-doped zone lies at a  
distance of at most 0.2 μm from the  
substrate surface; and wherein the maximum  
concentration of said dopant ions is at least 5  
x 10<sup>16</sup>/cm<sup>3</sup>. 90

5. An n-channel insulating layer field-  
effect transistor substantially as hereinbefore  
described with reference to and as shown in  
Figure 1 or Figure 2 of the drawing. 10

6. A method of producing a field-effect  
transistor as claimed in Claim 1, comprising  
the steps of depositing a p-conducting  
epitaxial silicon layer on an insulating  
substrate, producing an n<sup>+</sup>-doped source  
zone and an N<sup>+</sup>-doped drain zone in said  
silicon layer, implanting p-dopant ions in  
said epitaxial silicon layer within a region  
which underlies said source zone and extends  
laterally of said source zone by not more  
than 5 μm, implantation being effected  
through a mask so that no p-dopant ions are  
implanted in the remainder of said silicon  
layer. 11

7. A method as claimed in Claim 6,  
wherein the energy of the implanted dopant  
ions is such that the concentration maximum  
of the implanted dopant ions is situated at a  
distance of about 0.2 μm from the substrate  
surface. 12

8. A method as claimed in Claim 4 or  
Claim 5, wherein the maximum concentra- 13

tion of the implanted dopant ions is from  $2 \times 10^{16}$  to  $2 \times 10^{17}/\text{cm}^{-2}$ .

5 9. A method of producing a field-effect transistor as claimed in Claim 1, substantially as hereinbefore described with reference to Figure 3 of the drawing.

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Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1978.  
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from  
which copies may be obtained.

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## COMPLETE SPECIFICATION

1 SHEET

*This drawing is a reproduction of  
the Original on a reduced scale*